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Introduction

Overview

The Sealevel **OMG-ACB-II** Advanced Communications Board provides the PC with one high speed sync/async port. The **OMG-ACB-II** can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X.25, and High Speed Async.

What's Included

The **OMG-ACB-II** is shipped with the following items. If any of these items are missing or damaged, contact the supplier.

- (1) **OMG-ACB-II** Advanced Communications Board
- (1) 3.5″ ACB Developer Toolkit Diskette
- User Manual
- RS-232 Interface Chips (1488 & 1489)

Factory Default Settings

The **OMG-ACB-II** factory default settings are as follows:

Base Address	DMA Channel	IRQ	Electrical Specification
238	3	5	RS-422

To install the **OMG-ACB-II** using factory default settings, refer to Installation on page 6.

For your reference, record installed **OMG-ACB-II** settings below:

Base Address	DMA Channel	IRQ	Electrical Specification

Card Setup

The **OMG-ACB-II** contains several jumper straps for each port which must be set for proper operation.

Address Selection

The **OMG-ACB-II** occupies 8 consecutive I/O locations. The DIP-switch is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The **OMG-ACB-II** has a total of 8 I/O address selections, if more than one switch is closed the board will be non-functional. Leaving all eight switches open will disable the port

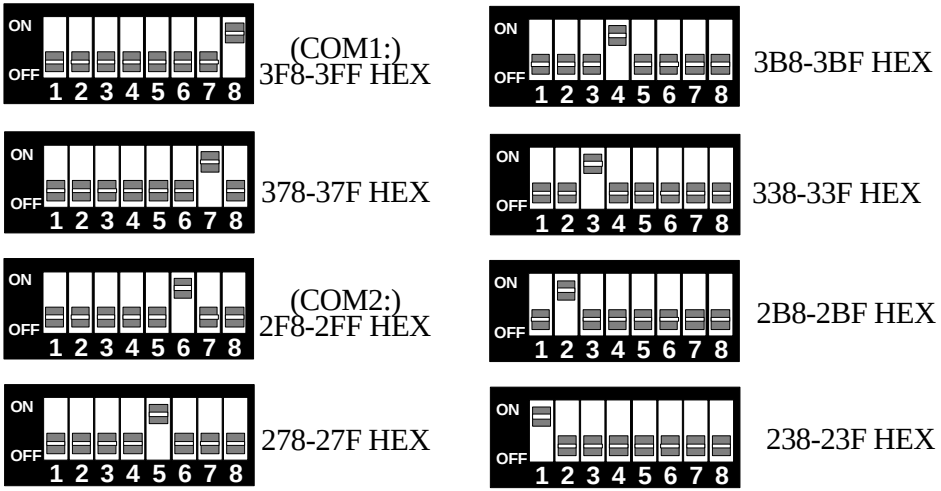


Figure 1 - DIP-Switch Illustration

Refer to Appendix A for common address contentions.

The relative I/O addresses of the **OMG-ACB-II** are as follows:

- Base+0 Channel A Data Port
- Base+1 Channel A Control Port
- Base+2 Channel B Data Port
- Base+3 Channel B Control Port

Interface Selection

Note: Only one interface can be selected at a time.

RS-232

The RS-232 option is selected when the RS-232 driver and receiver are installed at locations U17 (**1488**) and U11 (**1489**).

RS-422

The RS-422 option is installed when the RS-422/485 chips are installed at U6 (**75173**) and U7 (**75174**) and the RS-232 chips are removed.

RS-485

The RS-485 option is installed when the RS-422/485 chips are installed at U6 (**75173**) and U7 (**75174**). The output of the RS-422/485 driver is capable of being **Active** (enabled) or **Tri-State** (disabled) for RS-485 compatibility. Header E2 selects whether the RS-485 driver is enabled by the SCC signal **R**equest **T**o **S**end (RTS) or always enabled. With the jumper installed, RTS enables the driver (RS-485). Removing the jumper enables the driver regardless of RTS (RS-422). Refer to Appendix C for a detailed description of RS-422 and RS-485.

IRQ Selection

The **OMG-ACB-II** has an interrupt selection jumper that should be set prior to use. Consult the user manual for the application software being used to determine the proper setting. E1 & E9 select the interrupt request for the port. IRQ3, IRQ4, IRQ5, or no interrupt (removing all jumpers) can be selected, depending on jumper position. If no interrupt is desired, remove the jumper.

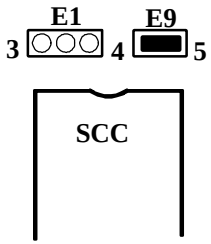


Figure 2 - Header E1 & E9, IRQ Selection (Shown in Factory Default)

DMA Channel Selection (Header E3)

The **D**irect **M**emory **A**ccess (DMA) Channel can be selected as Channel 1 or Channel 3. See the Appendix F for jumper position. If DMA is not used, these jumpers should be removed.

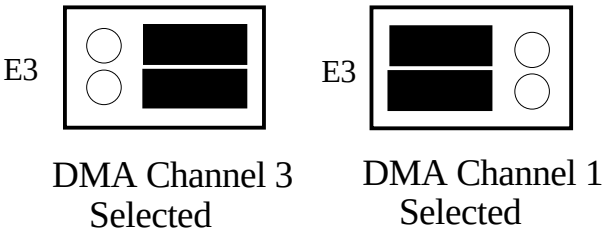


Figure 3 - Header E3 DMA Selection

DMA Enable (Header E7)

Header E7 selects whether the DMA Tri-State drivers are enabled, disabled or whether the RTS from Channel B is used to enable the DMA. The **'A'** position selects the **Always Enabled** mode. The **'B'** position selects **RTSB Enable**. Please refer to the Zilog SCC User's Manual for aid in programming Write Register 5 for RTSB. Removing the jumper disables the DMA drivers, and no DMA can be performed.

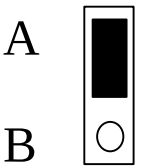


Figure 4 - Header E7 DMA Enable (Factory Default)

Miscellaneous I/O Pin Selection (Header E4)

Jumper block E4 allows the user to configure the **OMG-ACB-II** clock and miscellaneous I/O pins. Please refer to the following illustration for aid in configuring this header.

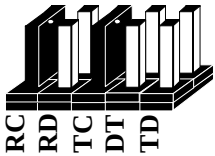


Figure 5 - Header E4 (Shown in Factory Default)

Input Pins

Choose only one of the following:

(pin 6 RS-232, pins 8 & 9 RS-422)

RC	Selects RXC pin as an input to the DB-25 connector
RD	Selects RDB pin as an input to the SCC

Output Pins

Choose only one of the following:

(pin 20 RS-232, pins 20 & 21 RS-422)

TC	Selects the TXC pin as an output to the DB-25 connector
DT	Selects the DTR pin as an output to the DB-25 connector
TD	Selects the TDB pin as an output to the DB-25 connector

Note: While the **OMG-ACB-II** is designed as a single port implementation of the SCC, the '**B**' channel **R**eceived **D**ata (RDB) and **T**ransmit **D**ata (TDB) are brought out to the DB-25 through Header E4; allowing the use of the second port on the SCC in a user definable two port application.

Installation

The **OMG-ACB-II** can be installed in any of the PC expansion slots. The **OMG-ACB-II** contains several jumper straps for each port which must be set for proper operation.

1. Turn off PC power. Disconnect the power cord.
2. Remove the PC case cover.
3. Locate an available slot and remove the blank metal slot cover.
4. Gently insert the **OMG-ACB-II** into the slot. Make sure the adapter is seated properly.
5. Replace the screw.
6. Replace the cover.
7. Connect the power cord.

Installation is complete.

Technical Description

The **OMG-ACB-II** utilizes the Zilog 85230 **S**erial **C**ommunications **C**ontroller (SCC). This chip features programmable baud rate, data format, interrupt control, and DMA control. Refer to the SCC User's Manual, the Zilog Datacom I/C Handbook and the ACB Developers Toolkit diskette for details on programming the SCC chip.

Features

- Sync/Async Communications using 85230 chip
- DMA supports data rates greater that one million bits per second
- Selectable port address
- Selectable IRQ Level (3,4,5)
- Selectable DMA Channel (1or 3)
- RS-232 or RS-422/485 interface
- Supports TD, RD, RTS, CTS, TXC, RXC Signals
- Jumper options for clock source
- Software programmable baud rate
- Software Toolkit provided
- Short card, DB-25 male connector

Programable Baud Rate Generator

The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 Megahertz (MHz). Other values may be substituted to achieve a higher or different baud rate, if required, by replacing the oscillator (U9) with a different part. Refer to the SCC User's Manual and the ACB Developers Toolkit diskette for baud rate divisors and programming information.

Connector Pin Assignments

RS-422

Signal	Name	Pin #	Mode
GND	Ground	7	
RX+	Receive Positive	12	Input
RX-	Receive Negative	13	Input
CTS+	Clear To Send Positive	10	Input
CTS-	Clear To Send Negative	11	Input
RXC+	Receive Clock Positive	8	Input
RXC-	Receive Clock Negative	9	Input
TX+	Transmit Positive	24	Output
TX-	Transmit Negative	25	Output
RTS+	Request To Send Positive	22	Output
RTS-	Request To Send Negative	23	Output
TXC+	Transmit Clock Positive	20	Output*
TXC-	Transmit Clock Negative	21	Output*
DTR+	Data Terminal Ready Positive	20	Output*
DTR-	Data Terminal Ready Negative	21	Output*

RS-232

Signal	Name	Pin #	Mode
GND	Ground	7	
RD	Receive Data	3	Input
CTS	Clear To Send	5	Input
RXC	Receive Clock**	6	Input
TD	Transmit Data	2	Output
RTS	Request To Send	4	Output
TXC	Transmit Clock**	20	Output*
DTR	Data Term Ready	20	Output*

* **Note:** These pins are determined by the Header E4 position setting.

** **Note:** These pins are not normally clock lines. Pins 15 and 17 are the normal RS-232 clock lines. If your equipment utilizes these clock signals, connect the TXC to pin 20, and the RXC to pin 6.

Specifications

Environmental Specifications

Specification	Operating	Storage
Temperature Range	0º to 50º C (32º to 122º F)	-20º to 70º C (-4º to 158º F)
Humidity Range	10 to 90% R.H. Non-Condensing	10 to 90% R.H. Non-Condensing

Manufacturing

- IPC 610-A Class-III standards are adhered to with a 0.1 visual A.Q.L. and 100% Functional Testing.
- All Omega Engineering Printed Circuit Boards are built to U.L. 94V0 rating and are 100% electrically tested. Printed Circuit Boards are solder mask over bare copper or solder mask over tin nickel.

Power Consumption

Supply line	+12 VDC	-12 VDC	+5 VDC
Rating	50 mA	50 mA	275 mA

Mean Time Between Failures (MTBF)

Greater than 150,000 hours. (Calculated)

Physical Dimensions

Board Length	4.6 inches	(11.68 cm)
Board Height including Goldfingers	4.2 inches	(10.66 cm)
Board Height excluding Goldfingers	3.9 inches	(9.906 cm)

Appendix A - Troubleshooting

An Advanced Communications Board Developers Toolkit Diskette is supplied with the Omega Engineering adapter and will be used in the troubleshooting procedures. By using this diskette and following these simple steps, most common problems can be eliminated without the need to call Technical Support.

1. Identify all I/O adapters currently installed in your system. This includes your on-board serial ports, controller cards, sound cards etc. The I/O addresses used by these adapters, as well as the IRQ (if any) should be identified.

2. Configure your Omega Engineering adapter so that there is no conflict with currently installed adapters. No two adapters can occupy the same I/O address.

3. Make sure the Omega Engineering adapter is using a unique IRQ. While the Omega Engineering adapter does allow the sharing of IRQ's, many other adapters (i.e. SCSI adapters and on-board serial ports) do not. The IRQ is typically selected via an on-board header block. Refer to the section on Card Setup for help in choosing an I/O address and IRQ.

4. Make sure the Omega Engineering adapter is securely installed in a motherboard slot.

5. Use the supplied diskette and User Manual to verify that the Omega Engineering adapter is configured correctly. The supplied diskette contains a diagnostic program 'SSDACB' that will verify if an adapter is configured properly. This diagnostic program is written with the user in mind and is easy to use. Refer to the 'README.txt' file on the supplied diskette for detailed instructions on using 'SSDACB'.

6. The following are known I/O conflicts:

    - The 278 and 378 settings may conflict with your printer I/O adapter.
    - 3B8-3BF cannot be used if a Monochrome adapter is installed.
    - 3F8-3FF is typically reserved for COM1:
    - 2F8-2FF is typically reserved for COM2:
    - 238-23F may conflict with a Bus Mouse

7. Please refer to your included diskette for any post production manual updates and application specific information.

8. Always use the Omega Engineering diagnostic software when Troubleshooting a problem. This will eliminate the software issue from the equation.

Appendix B - How To Get Assistance

Please refer to Appendix A - Troubleshooting prior to calling Technical Support.

1. Read this manual thoroughly before attempting to install the adapter in your system.
2. When calling for technical assistance, please have your user manual and current adapter settings. If possible, please have the adapter installed in a computer ready to run diagnostics.
3. Omega Engineering maintains a Home page on the Internet. Our home page address is www.omega.com. The latest software updates, and newest manuals are available via our FTP site that can be accessed from our home page.
4. Technical support is available Monday to Friday from 8:30 a.m. to 6:00 p.m. Eastern time. Technical support can be reached at (800)826-6342 x2295.

RETURN AUTHORIZATION MUST BE OBTAINED FROM OMEGA ENGINEERING BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING OMEGA ENGINEERING AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

Appendix C - Electrical Interface

RS-232

Quite possibly the most widely used communication standard is RS-232. This implementation has been defined and revised several times and is often referred to as RS-232 or EIA/TIA-232. It is defined by the EIA as the *Interface between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange*. The mechanical implementation of RS-232 is on a 25 pin D sub connector. RS-232 is capable of operating at data rates up to 20 Kbps at distances less than 50 ft. The absolute maximum data rate may vary due to line conditions and cable lengths. RS-232 often operates at 38.4 Kbps over very short distances. The voltage levels defined by RS-232 range from -12 to +12 volts. RS-232 is a single ended or unbalanced interface, meaning that a single electrical signal is compared to a common signal (ground) to determine binary logic states. A voltage of +12 volts (usually +3 to +10 volts) represents a binary 0 (space) and -12 volts (-3 to -10 volts) denotes a binary 1 (mark). The RS-232 and the EIA/TIA-574 specification defines two type of interface circuits, Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The Omega Engineering adapter is a DTE interface.

RS-422

The RS-422 specification defines the electrical characteristics of balanced voltage digital interface circuits. RS-422 is a differential interface that defines voltage levels and driver / receiver electrical specifications. On a differential interface, logic levels are defined by the difference in voltage between a pair of outputs or inputs. In contrast, a single ended interface, for example RS-232, defines the logic levels as the difference in voltage between a single signal and a common ground connection. Differential interfaces are typically more immune to noise or voltage spikes that may occur on the communication lines. Differential interfaces also have greater drive capabilities that allow for longer cable lengths. RS-422 is rated up to 10 Megabits per second and can have cabling 4000 feet long. RS-422 also defines driver and receiver electrical characteristics that will allow 1 driver and up to 32 receivers on the line at once. RS-422 signal levels range from 0 to +5 volts. RS-422 does not define a physical connector.

RS-485

RS-485 is backwardly compatible with RS-422; however, it is optimized for partyline or multi-drop applications. The output of the RS-422/485 driver is capable of being **Active** (enabled) or **Tri-State** (disabled). This capability allows multiple ports to be connected in a multi-drop bus and selectively polled. RS-485 allows cable lengths up to 4000 feet and data rates up to 10 Megabits per second. The signal levels for RS-485 are the same as those defined by RS-422. RS-485 has electrical characteristics that allow for 32 drivers and 32 receivers to be connected to one line. This interface is ideal for multi-drop or network environments. RS-485 tri-state driver (not dual-state) will allow the electrical presence of the driver to be removed from the line. The driver is in a tri-state or high impedance condition when this occurs. Only one driver may be active at a time and the other driver(s) must be tri-stated. The output modem control signal Request to Send (RTS) controls the state of the driver. Some communication software packages refer to RS-485 as RTS enable or RTS block mode transfer. RS-485 can be cabled in two ways, two wire and four wire mode. Two wire mode does not allow for full duplex communication, and requires that data be transferred in only one direction at a time. For half-duplex operation, the two transmit pins should be connected to the two receive pins (Tx+ to Rx+ and Tx- to Rx-). Four wire mode allows full duplex data transfers. RS-485 does not define a connector pin-out or a set of modem control signals. RS-485 does not define a physical connector.

Appendix D - Direct Memory Access

In many instances it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for higher rate data transfers, a special function called **D**irect **M**emory **A**ccess (DMA) was built into the original IBM PC. The DMA function allows the **OMG-ACB-II** (or any other DMA compatible interface) to read or write data to or from memory without using the Microprocessor. This function was originally controlled by the Intel 8237 DMA controller chip, but may now be a combined function of the peripheral support chip sets (i.e. Chips & Technology or Symphony chip sets).

During a DMA cycle the DMA controller chip is driving the system bus in place of the Microprocessor, providing address and control information. When an interface needs to use DMA it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA hold request to the Microprocessor. When the Microprocessor receives the hold request it will respond with an acknowledge to the DMA controller chip. The DMA controller chip then becomes a Bus Master providing the necessary control signals to complete a Memory to I/O or I/O to Memory transfer. When the data transfer is started an acknowledge signal (DACK) is sent by the DMA controller chip to the **OMG-ACB-II**. Once the data has been transferred to or from the **OMG-ACB-II**, the DMA controller returns control to the Microprocessor.

To use DMA with the **OMG-ACB-II** requires a thorough understanding of the PC DMA functions . The ACB Developers Toolkit demonstrates the setup and use of DMA with several source code and high level language demo programs. Please refer to the SCC User's Manual, the PC Technical Reference and the 8237 DMA controller chip specification for more information.

Appendix E - Asynchronous and Synchronous Communications

Serial data communications implies that individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync characters) are pre-defined and must correspond at both the transmitting and receiving ends. The techniques used for serial communications can be divided into two groups, *synchronous* and *asynchronous*.

When contrasting synchronous and asynchronous serial communications, the fundamental differences deal with how each method defines the beginning and the end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference between synchronous and asynchronous communications. The remainder of this section is devoted to detailing the differences between character framing and bit duration implemented in synchronous and asynchronous communications.

Asynchronous Communications

Asynchronous communications is the standard means of serial data communication for PC compatibles and PS/2 computers. The original PC was equipped with a communication or COM: port that was designed around an 8250 **U**niversal **A**synchronous **R**eceiver **T**ransmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communications are defined by a starting bit followed by a pre-defined number of data bits (5, 6, 7, or 8). The end of the character is defined by the transmission of a pre-defined number of stop bits (usual 1, 1.5 or 2). An extra bit used for error detection is often appended before the stop bits.

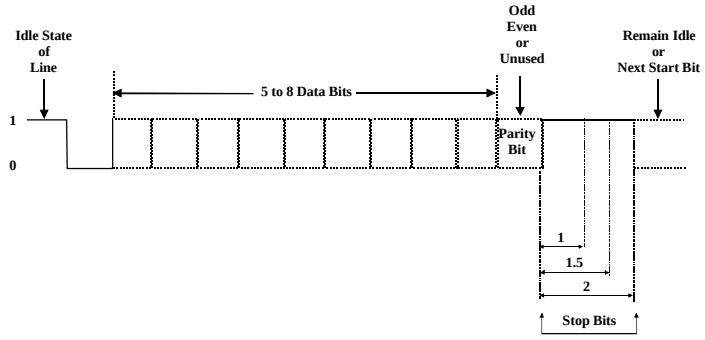


Figure 6 - Asynchronous Communications Bit Diagram

This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called (E)ven Parity or (O)dd Parity. Sometimes parity is not used to detect errors on the data stream. This is referred to as (N)o parity. Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communications by stating that each character is wrapped (framed) by pre-defined bits to mark the beginning and end of the serial transmission of the character. The data rate and communication parameters for asynchronous communications have to be the same at both the transmitting and receiving ends. The communication parameters are baud rate, parity, number of data bits per character, and stop bits (i.e. 9600,N,8,1).

Synchronous Communications

Synchronous communications is used for applications that require higher data rates and greater error checking procedures. Character synchronization and bit duration are handled differently than asynchronous communications. Bit duration in synchronous communications is not necessarily pre-defined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a pre-defined transmission. The source of the clock is predetermined and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communications, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates. Character synchronization with synchronous communications is also very different than the asynchronous method of using start and stop bits to define the beginning and end of a character. When using synchronous communications a pre-defined character or sequence of characters is used to let the receiving end know when to start character assembly.

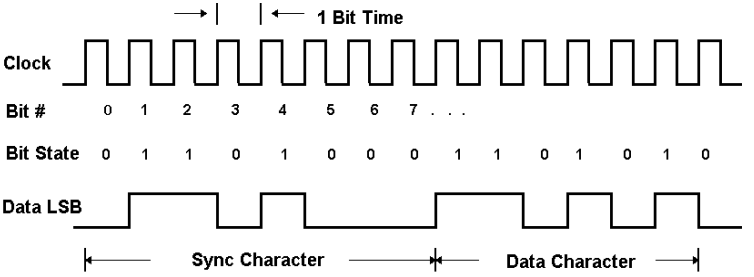
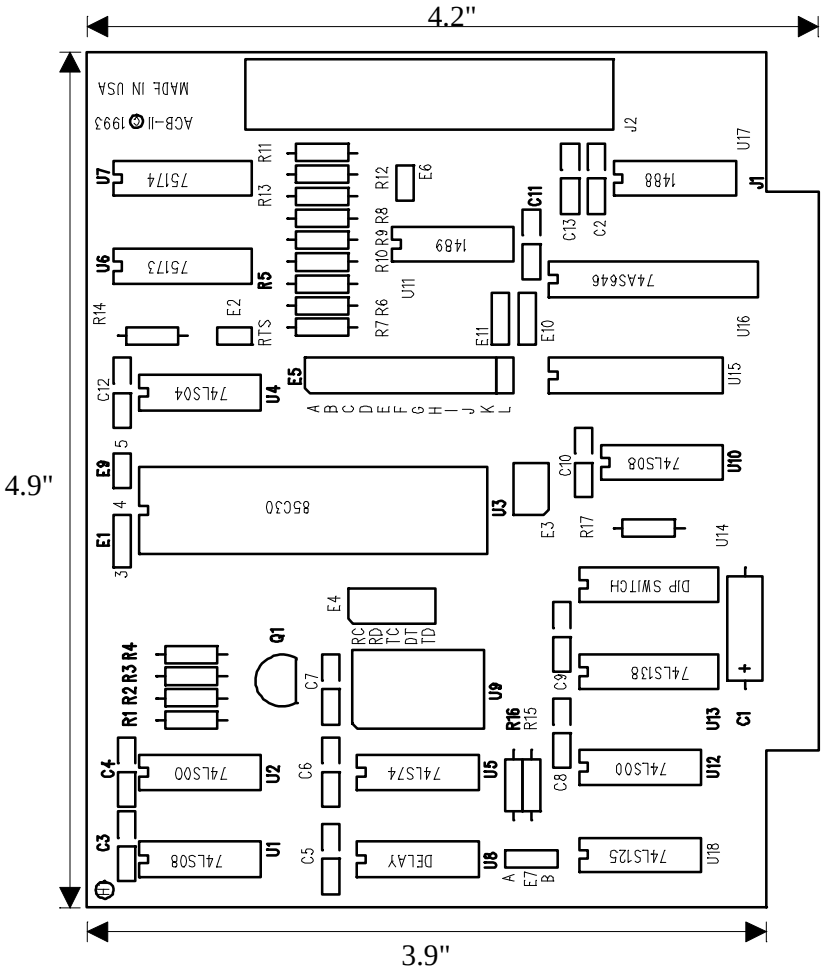


Figure 7 - Synchronous Communications Bit Diagram

This pre-defined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, let's assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the pre-defined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another pre-defined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, e.g., EOT). The actual sync flag and protocol varies depending on the sync format (SDLC, BISYNC, etc.).

For a detailed explanation of serial communications, please refer to the book *Technical Aspects of Data Communications* by John E. McNamara, published by Digital Press (DEC) 1982.

Appendix F - Silk-Screen



Appendix G - Compliance Notices

Federal Communications Commission Statement

FCC - This equipment has been tested and found to comply with the limits for Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in such case the user will be required to correct the interference at his own expense.

EMC Directive Statement

Products bearing the CE Label fulfill the requirements of the EMC directive (89/336/EEC) and of the low-voltage directive (73/23/EEC) issued by the European Commission.

To obey these directives, the following European standards must be met:

- **EN55022 Class A** - 'Limits and methods of measurement of radio interference characteristics of information technology equipment'
- **EN50082-1** - 'Electromagnetic compatibility - Generic immunity standard' Part 1 : Residential, commercial and light industry
- **EN60950 (IEC950)** - 'Safety of information technology equipment, including electrical business equipment'

Warning

This is a Class A Product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

Note: Double screen cabling is required to maintain compliance with EMC directives.

Warranty

Omega Engineering, Inc. warrants this product to be in good working order for a period of one year from the date of purchase. Should this product fail to be in good working order at any time during this period, Omega Engineering will, at it's option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Omega Engineering assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Omega Engineering will not be liable for any claim made by any other related party.

RETURN AUTHORIZATION MUST BE OBTAINED FROM OMEGA ENGINEERING BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING OMEGA ENGINEERING AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

Omega Engineering, Incorporated
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Technical Support is available from 8:30 a.m. to 6 p.m. Eastern time.
Monday - Friday

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